AMENDMENTS TO THE CLAIMS

1-2. (canceled)

3. (currently amended) A computer implemented method of determining aggressor-induced delay change in a victim net of a stage of an integrated circuit design, the stage including a victim net driver gate, a receiver gate and an interconnect network including a victim net and an aggressor net, comprising:

providing an input and output voltage dependent current model of the victim net ~~a~~ driver gate ~~of the victim net~~;

producing a model of a load presented to an output of the driver gate by the interconnect network;

producing a model of the ~~an~~ interconnect network of the stage, which can be used to propagate a waveform from an output of the driver gate ~~model~~ to an input of the ~~a victim net~~ receiver gate;

simulating behavior of the victim net during ~~determining~~ nominal (noiseless) transition by performing steps including, ~~delay in the stage by determining delay associated with the steps of,~~

providing a signal transition at an input of ~~to~~ the driver gate ~~model~~;

using the current model of the driver gate and the load model of the interconnect network to produce a nominal driver gate output waveform resulting from the provided input signal transition;

using the interconnect model to propagate the nominal ~~a~~ driver gate ~~model~~ output waveform~~, resulting from the provided signal transition,~~ from the driver gate ~~model~~ output to the receiver gate input;

simulating behavior of the victim net during ~~determining~~ noisy transition by performing steps including, ~~delay in the victim net by determining delay in the stage by determining delay associated with the steps of,~~

providing a signal transition at an input of the ~~to~~ driver gate ~~model~~;

providing an ~~at least one~~ aggressor-induced current waveform to an output of the driver gate ~~model~~;

using the current model of the driver gate and the load model of the interconnect network to produce a noisy driver gate output waveform resulting from the provided input signal transition and the aggressor-induced current waveform;

using the interconnect model to propagate the noisy ~~a~~ driver gate ~~model~~ output waveform~~, resulting from the provided signal transition and from the at least one aggressor-induced current waveform,~~ from the driver gate ~~model~~ output to the receiver gate input;

providing an ~~at least one~~ aggressor-induced voltage waveform to an input of the receiver gate; and

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition.~~ determining a difference between the nominal delay and noisy delay.~~

4. (original) The method of claim 3,

wherein the output current-dependent model of a driver of the victim net includes a ViVo model.

5. (currently amended) The method of claim 3,

wherein the output current-dependent model of a driver of the victim net includes a ViVo model; and

wherein the load ~~interconnect~~ model includes a Π-load model.

6. (previously amended) The method of claim 3 further including,

providing an input and output voltage dependent current model of the receiver gate;

wherein simulating behavior of the victim net during ~~determining~~ nominal transition ~~delay~~ further includes using at least the receiver gate current model to produce a nominal receiver gate output waveform resulting from the propagated nominal driver gate

~~propagating the propagated driver model~~ output waveform ~~to an output of the receiver~~; and

wherein simulating behavior of the victim net during ~~determining~~ noisy transition ~~delay in the stage~~ further includes using at least the receiver gate current model to produce a noisy receiver gate output waveform resulting from the propagated noisy driver gate ~~propagating the propagated driver~~ output waveform and the at least one aggressor-induced voltage waveform provided to the receiver model input ~~and the provided at least one aggressor induced waveform to an output of the receiver~~.

7-12. (canceled)

13. (currently amended) An article of manufacture including a computer readable medium encoded with an information structure representing ~~A model of~~ a driver ~~gate~~ circuit, the information structure comprising:

a current model that associates instantaneous values of input node voltage, output node voltage and output node current of the driver ~~gate~~ circuit;

a model of capacitance between an input node and an output node of the driver ~~gate~~ circuit; and

a model of capacitance between the output node of the driver ~~gate~~ circuit and a ground potential.

14. (currently amended) The article of manufacture ~~model~~ of claim 13 wherein,

the driver ~~gate~~ circuit current model includes a model of at least one channel connected component of the driver ~~gate~~ circuit.

15. (currently amended) The article of manufacture ~~model~~ of claim 13 wherein,

the driver ~~gate~~ circuit current model includes a model of a last channel connected component of the driver ~~gate~~ circuit.

16. (currently amended) The article of manufacture ~~model~~ of claim 13 wherein,

the driver ~~gate~~ circuit current model includes only a model of a last channel connected component of the driver ~~gate~~ circuit.

17. (currently amended) The article of manufacture ~~model~~ of claim 13, further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the driver ~~gate~~.

18. (currently amended) The article of manufacture ~~model~~ of claim 13,

wherein the driver ~~gate~~ circuit current model includes only a model of a last channel connected component of the driver ~~gate~~ circuit; and further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the driver ~~gate~~.

19. (currently amended) An article of manufacture including a computer readable medium encoded with an information structure representing ~~A model of~~ a driver ~~gate~~ circuit, the information structure comprising:

a current model that associates instantaneous values of driver ~~gate~~ circuit input node voltage, driver ~~gate~~ circuit output node voltage and driver ~~gate~~ circuit output node current;

a model of miller capacitance of the output node of the driver ~~gate~~ circuit; and

a model of ground capacitance of the output node of the driver ~~gate~~ circuit.

20. (currently amended) The article of manufacture ~~model~~ of claim 19 further including:

information concerning slew rate on the input node of the at least one component characterized as a function of slew rate on at least one input node of the driver ~~gate~~.

21. (currently amended) An article of manufacture including a computer readable medium encoded with computer instructions for performing a ~~A~~ circuit simulation process ~~to produce a current model of a gate circuit~~ comprising the steps of:

for each of a plurality of different pairs of first and second DC voltage values,

sensitizing an input node of a cell model of the driver ~~gate~~ circuit with a first DC voltage value; and

sensitizing an output node of the cell model with a second DC voltage value; and

generating a value of current drawn by the output node of the cell model based upon the provided first DC voltage value and the provided second DC voltage value.

22. (currently amended) The article of manufacture ~~method~~ of claim 21, the process further including:

producing a table representing respective associations among respective pairs of first DC voltage values and second DC voltage values and respective current values generated based upon such respective pairs.

23. (currently amended) The article of manufacture ~~method~~ of claim 21 wherein,

each respective first DC value includes a constant DC value; and

each respective second DC value includes a constant DC value.

24. (currently amended) The article of manufacture ~~method~~ of claim 21 wherein,

the driver ~~gate~~ circuit model includes a model of at least one channel connected component of the driver ~~gate~~ circuit.

25. (currently amended) The article of manufacture ~~method~~ of claim 21 wherein,

the driver ~~gate~~ circuit model includes a model of a last channel connected component of the driver ~~gate~~.

26. (currently amended) The article of manufacture ~~method~~ of claim 21 wherein,

the driver ~~gate~~ circuit model includes only a model of a last channel connected component of the driver ~~gate~~.

27. (currently amended) The article of manufacture ~~method~~ of claim 21, the process further including:

producing a model of capacitance between the input node of the and the output node of the driver ~~gate~~ circuit; and

producing a model of capacitance between the output node of the driver ~~gate~~ circuit and a ground potential.

28. (currently amended) The article of manufacture ~~method~~ of claim 21, the process further including:

determining capacitance between the input node and the output node of the driver ~~gate~~ circuit through transient analysis; and

determining capacitance between the output node the driver ~~gate~~ circuit and a ground potential through transient analysis.

29. (currently amended) The article of manufacture ~~method~~ of claim 21 [[31]], the process further including:

determining a slew rate on an input node of the cell model of the driver ~~gate~~ circuit characterized as a function of slew rate on an input node of the cell model of the driver ~~gate~~ circuit.

30. (currently amended) The article of manufacture ~~method~~ of claim 21 [[31]],

wherein the driver ~~gate~~ circuit model includes only a model of a last channel connected component of the driver ~~gate~~; further including:

determining a slew rate on an input node of the cell model characterized as a function of slew rate on an input node of the cell model of the driver ~~gate~~ circuit.

31. (currently amended) An article of manufacture including a computer readable medium encoded with a ~~data structure representing a~~ current model of a driver ~~gate~~ circuit, the current model ~~data structure~~ associating input voltage values, output voltage values and current values, the current model ~~data structure~~ produced by a process including the steps of:

for each of a plurality of different pairs of first and second DC voltage values,

sensitizing an input node of a cell model representing the driver ~~gate~~ circuit with a first DC voltage value; and

sensitizing an output node of the cell model with a second DC voltage value; and

generating a value of current drawn by the output node of the cell model based upon the provided first DC voltage value and the provided second DC voltage value.

32. (previously presented) The article of claim 31 wherein the process further includes the step of:

producing a table representing the respective associations among first DC voltage values, second DC voltage values and current values.

33. (previously presented) The article of claim 31 wherein,

each respective first DC value includes a constant DC value; and

each respective second DC value includes a constant DC value.

34. (currently amended) An article of manufacture including a computer readable medium encoded with instructions for performing a ~~A~~ method of simulating aggressor-induced behavior of a driver ~~gate~~ circuit and an interconnect network driven by the driver ~~gate~~ circuit, the method comprising:

providing a voltage signal transition on an input of a current model representing the driver ~~gate~~ circuit, the current model associating instantaneous values of input voltage, output voltage and output current of the driver ~~gate~~ circuit;

providing an aggressor induced current waveform on a node interconnecting an output of the current model and a load model representing the interconnect network, the load model approximating output point admittance of the interconnect network; and

using the current model and the load model to produce a voltage waveform on the output of the current model based upon the received input voltage signal transition and the received aggressor induced waveform.

35. (currently amended) The article of manufacture ~~method~~ of claim 34,

wherein the current model includes a model of capacitance associated with the driver circuit ~~of the at least one component~~.

36. (currently amended) The article of manufacture ~~method~~ of claim 34,

wherein the current model includes a model of miller capacitance associated with the driver circuit ~~of the at least one component~~; and

wherein the current model includes a model of ground ~~gate~~ capacitance associated with the driver circuit ~~of the at least one component~~.

37. (currently amended) The article of manufacture ~~method~~ of claim 34 wherein, the load model includes a Π-model.

38. (currently amended) The article of manufacture ~~method~~ of claim 34 wherein, the at least one component comprises a channel connected component.

39. (currently amended) The article of manufacture ~~method~~ of claim 34 wherein, the current model includes a model of a last channel connected component of the driver ~~gate~~.

40. (currently amended) A computer implemented method of determining ~~simulating~~ aggressor-induced delay change in a victim net in an integrated circuit design, the victim net including a driver circuit ~~, a receiver circuit~~ and an interconnect network between the driver circuit and a ~~the~~ receiver circuit, the method comprising:

simulating behavior of the victim net during ~~determining~~ nominal (noiseless) transition by performing steps including, ~~delay in the victim net by determining delay associated with a signal propagation process comprising,~~

providing a voltage signal transition on an input of ~~a current model of~~ the driver circuit;

using a driver circuit current model and ~~in which a node interconnects an output of the current model and~~ a load model ~~representing the interconnect network, the load model~~ approximating output point admittance of the interconnect network presented to an output of the driver circuit, to produce a nominal driver circuit output voltage waveform resulting from the provided transition signal; and

using a computational model of the interconnect network to propagate the nominal driver circuit output ~~a~~ voltage waveform to an input of ~~a model of~~ the receiver circuit ~~in response to the current model nominal output voltage waveform~~;

simulating behavior of the victim net during ~~determining~~ noisy transition by performing steps including, ~~delay in the victim net by determining delay associated with a signal propagation process comprising,~~

providing a voltage signal transition on the input of the ~~current model of~~ driver circuit;

providing an aggressor induced current waveform to the output node of the driver circuit ~~current model~~;

using the driver circuit current model and ~~that interconnects the output of the current model~~ and the load model ~~that interconnects the output of the current model and the load model representing the interconnect network, so as~~ to produce a ~~current model~~ noisy driver circuit output voltage waveform resulting from the provided transition signal and the aggressor-induced current waveform; and

using the computational model of the interconnect network to propagate the noisy ~~a~~ output voltage waveform to an input of ~~a model of~~ the receiver circuit ~~in response to the current model noisy output voltage waveform~~; and

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition.~~determining a difference between the nominal delay and noisy delay.~~

41. (previously presented) The method of claim 40,

wherein the current model includes a model of capacitance of the driver circuit.

42. (previously presented) The method of claim 40,

wherein the current model includes a model of miller capacitance of the driver circuit; and

wherein the current model includes a model of gate capacitance of the driver circuit.

43. (previously presented) The method of claim 40 wherein,

the load model includes a Π-model.

44. (previously presented) The method of claim 40 wherein,

the current model includes a model of a last channel connected component of the driver circuit.

45. (previously presented) The method of claim 40 wherein,

the computational model of the interconnect network includes one or more transfer functions that relate a signal on a driver circuit output node to a signal on a receiver circuit input node.

46. (previously presented) The method of claim 40 wherein,

the model of the receiver includes a current model.

48. (currently amended) The method of claim 40 wherein,

the driver circuit current model associates instantaneous values of input node voltage, output node voltage and output node current of the driver ~~gate~~ circuit.

49. (currently amended) The method of claim 40 wherein,

the driver circuit current model associates instantaneous values of input node voltage, output node voltage and output node current of the driver ~~gate~~ circuit; and

the driver circuit current model includes a model of capacitance between an input node and an output node of the driver ~~gate~~ circuit; and

the driver circuit current model includes a model of capacitance between the output node of the driver ~~gate~~ circuit and a ground potential.

50. (new) The method of claim 3,

wherein simulating behavior of the victim net during nominal (noiseless) transition further includes,

using a current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated nominal driver gate output waveform; and

wherein simulating behavior of the victim net during noisy transition further includes, using the current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated noisy driver gate output waveform and the aggressor-induced voltage waveform to an input of the receiver gate.

51. (new) The method of claim 3 further including:

precomputing the current waveform through a driver gate pin induced by a transitioning aggressor net to produce the aggressor-induced current waveform; and

precomputing the voltage waveform at a receiver pin induced by the transitioning aggressor net to produce the aggressor-induced voltage waveform.

52. (new) The method of claim 3,

wherein providing a model of the interconnect network includes providing a computational model that includes a transfer function that includes an admittance matrix that relates voltage on one port of the matrix to current on another port of the matrix;

using the computational model to compute the aggressor-induced current waveform; and

using the computational model to compute the aggressor-induced voltage waveform.

53. (new) The method of claim 3,

wherein the load model approximates output point admittance of the interconnect network.

54. (new) The method of claim 3,

wherein the model of the load represents a ∏-load model and further includes a model of capacitance of the driver gate output pin.

55. (new) The method of claim 40,

wherein simulating behavior of the victim net during nominal transition further includes,

using a receiver circuit current model of the receiver circuit to produce a receiver circuit nominal output waveform, resulting from the propagated nominal output voltage waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

using the receiver circuit current model to produce a receiver circuit noisy output waveform, resulting from the propagated noisy output voltage waveform.

56. (new) The method of claim 40,

wherein simulating behavior of the victim net during nominal transition further includes,

using a receiver circuit current model of the receiver circuit to produce a receiver circuit nominal output waveform, resulting from the propagated nominal output voltage waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

providing an aggressor-induced voltage waveform at an input of the receiver circuit; and

using the receiver circuit current model to produce a receiver circuit noisy output waveform, resulting from the propagated noisy output voltage waveform and the aggressor-induced voltage waveform at an input of the receiver ciruit.

57. (new) An article of manufacture including a computer readable medium encoded with instructions for performing a method of determining aggressor-induced delay change in a victim net of a stage of an integrated circuit design, the stage including a victim net driver gate, a receiver gate and an interconnect network including a victim net and an aggressor net, the method comprising:

simulating behavior of the victim net during nominal (noiseless) transition by performing steps including,

providing a signal transition to an input of the driver gate;

using a current model of the driver gate and a load model of the interconnect network to produce a nominal driver gate output waveform resulting from the provided input signal transition;

using a model of the interconnect network to propagate the nominal driver gate output waveform from the driver gate output to the receiver gate input;

simulating behavior of the victim net during noisy transition by performing steps including,

providing a signal transition at the input of the driver gate;

providing at least one aggressor-induced current waveform to an output of the driver gate;

using the current model of the driver gate and the load model of the interconnect network to produce a noisy driver gate output waveform resulting from the provided input signal transition and the at least one aggressor-induced current waveform provided to the driver gate output;

using the interconnect model to propagate the noisy driver gate output waveform from the driver gate output to the receiver gate input;

providing at least one aggressor-induced voltage waveform to an input of the receiver gate; and

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition.

58. (new) The article of claim 57, wherein the method further including:

providing as the current model, an input and output voltage dependent current model of the driver gate;

producing as the load model, a model of a load presented to an output of the driver gate by the interconnect network; and

producing as the model of the interconnect network, a computational model of the interconnect network that includes one or more transfer functions that relate a signal on a driver gate output node to a signal on a receiver gate input node.

59. (new) The article of claim 57,

wherein simulating behavior of the victim net during nominal (noiseless) transition further includes,

using a current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated nominal driver gate output waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

using the current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated noisy driver gate output waveform.

60. (new) The article of claim 57,

wherein simulating behavior of the victim net during nominal (noiseless) transition further includes,

using a current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated nominal driver gate output waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

providing an aggressor-induced voltage waveform at an input of the receiver gate; and

using the current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated noisy driver gate output waveform and the aggressor-induced voltage waveform at an input of the receiver gate.

61. (new) An article of manufacture including a computer readable medium encoded with instructions for performing a method of determining aggressor-induced delay change in a victim net of a stage of an integrated circuit design, the stage including a victim net driver gate, a receiver gate and an interconnect network including the victim net and an aggressor net,, the method comprising:

simulating behavior of the victim net during nominal (noiseless) transition by performing steps including,

providing a voltage signal transition on an input of a the driver gate;

using a current model of the driver gate and a load model representing the interconnect network, the load model approximating output point admittance of the interconnect network, to produce a nominal driver gate output voltage waveform in response to the input voltage transition; and

using a computational model of the interconnect network to propagate the nominal driver gate output voltage waveform to an input of the receiver gate;

simulating behavior of the victim net during noisy transition by performing steps including,

providing a voltage signal transition to the input of the driver gate;

providing an aggressor induced current waveform to an output of the driver gate;

using the current model of the driver gate and the load model to produce a noisy driver gate output voltage waveform in response to the input voltage transition and the aggressor induced current waveform; and

using the computational model of the interconnect network to propagate the noisy driver gate output voltage waveform to an input of the receiver gate; and

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition.

62. (new) The article of manufacture of claim 61,

wherein simulating behavior of the victim net during nominal (noiseless) transition further includes,

using a current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated nominal driver gate output waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

using the current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated noisy driver gate output waveform.

63. (new) The article of claim 61,

wherein simulating behavior of the victim net during nominal (noiseless) transition further includes,

using a current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated nominal driver gate output waveform; and

wherein simulating behavior of the victim net during noisy transition further includes,

providing an aggressor-induced voltage waveform at an input of the receiver gate; and

using the current model of the receiver gate to produce a receiver gate output waveform resulting from the propagated noisy driver gate output waveform and the aggressor-induced voltage waveform at an input of the receiver gate.

64. (new) The article of manufacture of claim 61 wherein the information structure further includes:

a model of a load presented by an interconnect network associated with an output of the driver model.

65. (new) The article of manufacture of claim 64,

wherein the load model approximates output point admittance of the interconnect network.

66. (new) The article of manufacture of claim 64,

wherein the model of the load includes a $\prod$-model.